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Docket No.: 060188-0685

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Osamu MATSUI, et al.	:	Confirmation Number: 9750
Application No.: 10/690,705 Patent No. 6,975,003 B2	:	Group Art Unit: 2811
Filed: October 23, 2003 Issued: December 13, 2005	:	Examiner: Gene M. Munson

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop CERTIFICATE OF CORRECTION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring correction in order to conform the Official Record in the application.

The error noted is set forth on the attached copy of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, on the title page and at the top of Column 1 in the specification, Item "(54)", change the title from SEMICONDUCTOR CMOS SOI" to -- **SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME** --. Copies of the Declaration and Issue Fee transmittal form, showing the correct version of the title are enclosed.

In addition, on the title page, Item "(56) **References Cited**", below the listing of "6,313,508 B1 11/2001 Kobayashi", insert the following: -- FOREIGN PATENT DOCUMENTS 3111947

9/2000 (JP) --. This patent is mentioned on Page 1, line 11, of the specification, a copy of which is attached.

The change requested herein occurred as a result of printing the Letters Patent and the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Accordingly, Applicants request issuance of the Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

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Date: March 17, 2006

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6975003 B2

DATED : December 13, 2005

INVENTOR(S): Osamu MATSUI, et al.

It is certified that error appears in the above-identified patent and that said Letter Patent is hereby corrected as shown below:

TITLE PAGE,

Item "(54)" and top of Column 1,

change "SEMICONDUCTOR CMOS S0I" to -- SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME --.;

Item "(56) **References Cited**", following the listing "6,313,508 B1 11/2001 Kobayashi", insert

-- FOREIGN PATENT DOCUMENTS

3111947 9/2000 (JP) –

MAR 21 2006

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 03/18/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY LLP
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

CUSTOMER NO.: 20277

Note: A certificate of mailing can only be used for domestic mailings of Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,705	10/23/2003	Osamu Matsui	60188-685	9750

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	06/20/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
MUNSON, GENE M	2811	257-351000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McDERMOTT WILL &
2 EMERY LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): OSAKA, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Governm

4a. The following fee(s) are enclosed:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies Four

4b. Payment of Fee(s):
- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment Deposit Account Number 500417 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 04/18/2005

Typed or printed name Michael E. Fogarty Registration No. 36,139

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Docket No. _____

COMBINED DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
___, the specification of which

(check one) X is attached hereto.

___ was filed on _____ as Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
2002-309319 (Number)	JAPAN (Country)	24/10/2002 (Day/Month/Year Filed)	X Yes __ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	__ Yes __ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	__ Yes __ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Paul Devinsky (Reg. No. 28,553); Edward E. Kubasiewicz (Reg. No. 30,020), Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); and Wilhlem F. Gadiano (Reg. No. 37,136).

Please address all correspondence and telephone calls to:

Jack Q. Lever, Jr.
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(202) 756-8000

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishableby fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Osamu MATSUI

Inventor's signature Osamu Matsui Date October 20, 2006

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Inventor's signature Yoshinobu Sato Date October 20, 2003
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* City and State, or City and Country for foreign inventors

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a method for fabricating the device, and more particularly relates to a semiconductor device in which MOS transistors are formed on an SOI (silicon on insulator) substrate, and a method for fabricating the device.

Conventionally, semiconductor devices that have a MOS structure, in which a Pch-transistor and an Nch-transistor are formed on an SOI substrate, have found a wide variety of applications. Particularly, the patent document **1** (Japanese Laid-Open Patent Publication No. 3111947 (FIG. **1** and descriptions thereof)) discloses a semiconductor device for use in a driving circuit in a plasma display, which semiconductor device employs MOS transistors with an offset structure in order to obtain a high breakdown-voltage characteristic.

FIG. **6** is a cross-sectional view of a conventional semiconductor device that includes transistors with an offset structure as the semiconductor device disclosed in the patent document **1** does. In the semiconductor device shown in FIG. **6**, an N-channel transistor and a P-channel transistor, each being a MOS transistor with an offset structure, are formed on a common SOI substrate.

As shown in FIG. **6**, the conventional semiconductor device includes a buried oxide film **102**, a semiconductor layer **103**, trench isolation regions **104**, field oxide films **105a** through **105d**, and an interlevel dielectric film **106**. The buried oxide film **102** is formed on a supporting substrate (silicon substrate) **101**. The semiconductor layer **103** is formed on the buried oxide film **102**. The trench isolation regions **104** are provided to divide the semiconductor layer **103** into a plurality of active regions **103a**, **103b**, ···. The field oxide